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TRANSMITTAL FORM

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First Named Inventor	Dean A. Klein
Group Art Unit	2614
Examiner Name	Trang U. Tran
Attorney Docket Number	2269-5686US (MUEI-0059.01/US)

ENCLOSURES *(check all that apply)*

- [x] Postcard receipt acknowledgment (attached to the front of this transmittal)
- [x] Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- [ ] Preliminary Amendment
- [ ] Response to Restriction Requirement/Election of Species Requirement dated
- [ ] Amendment in response to office action dated
- [ ] Amendment under 37 C.F.R. § 1.116 in response to final office action dated
- [ ] Additional claims fee - Check No. in the amount of $
- [ ] Letter to Chief Draftsman and copy of FIGS. with changes made in red
- [ ] Transmittal of Formal Drawings
- [ ] Formal Drawings (sheets)
- [ ] Information Disclosure Statement, PTO/SB/08A (08-00); [ ] copy of cited references
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Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

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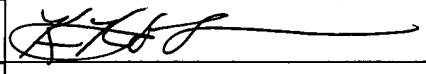
Firm *or* Individual name	Kevin K. Johanson Registration No. 38,506
Signature	
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Dean A. Klein

Serial No.: 09/048,933

Filed: March 26, 1998

For: METHOD FOR ASSISTING VIDEO COMPRESSION IN A COMPUTER SYSTEM

Confirmation No.: 4879

Examiner: Trang U. Tran

Group Art Unit: 2614

Attorney Docket No.: 2269-5686US
(MUEI-0059.01/US)

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BRIEF ON APPEAL

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Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted pursuant to 37 C.F.R.§ 41.37 and in the format required by 37 C.F.R. § 41.37(c) and with the fee required by 37 C.F.R. § 41.20(b)(2):

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., the assignee of the pending application as recorded at Reel 010763, Frame 0572 with the United States Patent and Trademark Office.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellant, Appellant's representative, nor Assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF CLAIMS

Claims 1 through 9 and 12 through 19 are pending in the application.

Claims 10, 11 and 20 were previously cancelled.

No claims were previously withdrawn.

Claims 1 through 9 and 12 through 19 stand rejected.

No claims are allowed.

The rejections of claims 1 through 9 and 12 through 19 are being appealed.

(4) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed on June 2, 2005. On August 2, 2005, an amendment was filed under 37 C.F.R. § 1.116 in response to the Examiner's remarks in the Final Office Action of June 2, 2005. No amendments to the claims were proposed in the Remarks. An Advisory Action mailed on August 24, 2005 found the arguments unpersuasive and maintained the rejection of claims 1 through 9 and 12 through 19.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

The invention presently claimed in pending claims 1 through 9 and 12 through 19 relates to compressing video data, and more specifically to a method that provides assistance to a computer system in compressing a stream of video data on-the-fly, as the video data streams into the computer system. (Specification, page 1, line 23 through page 2, line 2). Specifically, the invention presently claimed is a method for compressing video data in a computer system, in various embodiments not found in the prior art, for receiving video data and compressing video data to produce compressed video data. (Specification, page 3, lines 6-18).

In one embodiment of the present invention as claimed with respect to independent claim 1, a method is provided for compressing video data in a computer system. (Specification, page 3, lines 6-9). The method includes receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame. (FIGS. 2 and 3; Specification, page 8, lines 18-23). The core logic chip computes a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input. (FIG. 3; Specification, page 8, lines 4-6). The method further includes storing the difference frame directly from the core logic chip to the system memory in the computer system via a dedicated memory interface therebetween. (FIGS. 2 and 3; Specification, page 7, lines 17-21). The processor retrieves the difference frame directly from the system memory via the core logic chip using a dedicated processor interface therebetween. (FIGS. 2 and 3; Specification, page 7, lines 19-21).

In another embodiment of the present invention as claimed with respect to independent claim 13, a method is provided for compressing video data in a computer system. (Specification, page 3, lines 6-9). The method includes receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame. (FIGS. 2 and 3; Specification, page 8, lines 18-23). The core logic chip computes a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input. (FIG. 3; Specification, page 8, lines 4-6). The method further includes storing the difference frame directly from the core logic chip to the system memory in the computer system via a dedicated memory interface therebetween. (FIGS. 2 and 3; Specification, page 7, lines 17-21). A current video frame is also directly stored from the core logic chip into the system memory using a dedicated processor interface therebetween. (Specification, page 11, lines 3-6). The processor retrieves the difference frame directly from the system memory via the core logic chip using a dedicated processor interface therebetween. (FIGS. 2 and 3; Specification, page 7, lines 19-21).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Whether claims 1 through 3, 5 through 9 and 12 are patentable under 35 U.S.C. § 103(a) over Owen et al. (U.S. Patent No. 6,427,194) in view of Dea (U.S. Patent No. 5,469,208) and further in view of Melo et al. (U.S. Patent No. 6,040,845).

(2) Whether claims 4 and 13 through 19 are patentable under 35 U.S.C. § 103(a) over Owen et al. (U.S. Patent No. 6,427,194) in view of Dea (U.S. Patent No. 6,040,845), Melo et al. (U.S. Patent No. 6,040,845), and further in view of Abramatic et al. (U.S. Patent No. 4,546,383).

(7) ARGUMENT

A. Authorities Relied Upon

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

It is improper to combine references where the references teach away from their combination. MPEP § 2145 (citing *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)).

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert.denied*, 469 U.S. 851 (1984).

The Federal Circuit has repeatedly cautioned against employing hindsight by using the applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teaching of the prior art. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.*, 840 F.2d 902, 907, 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988).

B. Summary of Cited Prior Art

Owen teaches or suggests an electronic system that contains a first device and video and/or audio decompression and/or compression device capable of operating in real time. (Owen, col. 4, lines 60-63). Both the first device and the video and/or audio decompression and/or compression device require access to a memory. (Owen, col. 4, lines 63-65). In Owen, (i) the encoding/decoding device 80 (presumably where any difference frame calculation could occur), (ii) the main memory 168 and (iii) accelerator graphics port 160 are all coupled together using a single interface, namely memory bus 167. (Owen, FIG. 3; col. 9, line 61 through col. 10, line 12). Also in Owen, any computing of a difference frame (not explicit in Owen) would need to occur in decoder/encoder 80 (FIG. 3) which is isolated by a single interface, namely memory bus 167 (Owen, FIG. 3).

Dea teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204

and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Dea, col. 5, lines 40-42). The Dea architecture includes a difference block 220 which is only accessible by way of bus interface 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which receive their data over a single bus interface 200. (Dea, FIGS. 1 and 2; col. 5, lines 38-47).

Melo teaches or suggests a computer having multiple buses including a CPU bus and several peripheral buses. (Melo, col. 4, lines 19-21). A CPU bus connects a CPU or processor 12 to a bus interface unit or north bridge 14 which also provides an interface between components clocked at dissimilar rates. (Melo, col. 4, lines 22-30). The north bridge may also contain a memory controller which allows data communication to and from system memory 18. (Melo, col. 4, lines 30-32). The north bridge 14 may also include a graphics port to allow connection to a graphics accelerator 20. (Melo, col. 4, lines 33-35). The graphics accelerator 20 requests data from system memory 18 via the memory controller within north bridge 14 resulting in a dedicated graphics bus [AGP bus of FIG. 1] having rapid retrieval of data from system memory 18. (Melo, col. 4, lines 46-49).

Abramatic teaches or discloses a method of transmitting visual information over a telecommunications network. (Abramatic, col. 2, lines 33-35). The method discriminates on the basis of differences in brightness between neighboring points in an image in order to obtain a sequence of electric signals representative of the contours in the original image. (Abramatic, col. 2, lines 41-46).

C. Arguments for Patentability of Claims 1 through 3, 5 through 9 and 12

(1) *Claims 1 through 3, 5 through 9 and 12 are patentable because the cited references do not teach or suggest all of the claim limitations.*

Specifically, Appellant's independent claim 1 recites:

> 1. A method for compressing video data in a computer system comprising:
> ***receiving a current video frame at a dedicated video input*** of a core logic chip in the computer system ***directly from a video source originating the video frame***, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
> ***computing*** at the core logic chip ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;
> ***storing the difference frame directly*** from the core logic chip to the system memory in the computer system ***via a dedicated memory interface*** therebetween; and
> the processor retrieving the difference frame directly from the system memory via the core logic chip using a dedicated processor interface therebetween to complete compression of the video data. (Emphasis added.)

In rejecting 1-3, 5-9 and 12, it is asserted that:

Dea discloses in col. 9, lines 60-63 that "The encoding pathway receives a previous image and a current image into buffers 204, 206 respectively. The difference between the two may be applied by frame difference block 220 to selectable discrete cosine transform block 230". It is noted that previous image is current image delayed by one image. ***Thus, the claimed "receiving a current video frame at a dedicated video input of a core logic chip ... directly from a video source originating the video frame ..." is anticipated by buffer 206 of Dea and the claimed "computing*** at the core logic chip ***a difference*** from the current video frame and a previous video frame ***as the current video frame streams into the dedicate video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, ..."

> ***is anticipated by frame different block 220 of Dea*** because the previous image is the current image delay by one image. (Office Action, pp. 2-3.; emphasis added).

Appellant respectfully disagrees with the characterization of the teachings of Dea and Owen. Appellant's computing of a difference frame is performed in a pipelined configuration, specifically via a receiving input, namely the "dedicated video input" and a storing output, namely "a dedicated memory interface." Specifically, Appellant's invention as claimed in independent claim 1 is drawn to "***receiving a current video frame at a dedicated video input*** ... ***directly from a video source originating the video frame***, ...; ***computing*** ... ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** ...; ***storing the difference frame directly*** ... ***via a dedicated memory interface*** ...."

In contrast, in the ***Owen reference***, any computing of a difference frame would need to occur in decoder/encoder 80 (FIG. 3) which is isolated by a ***single interface***, namely memory bus 167 (FIG. 3). Similarly and also in contrast to Appellant's invention as claimed, in the ***Dea reference*** teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of a ***single interface*** 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored and retrieved from memory 114.

The Office Action cites Melo et al for "teach[ing] that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be

partially considered as an AGP compliant target . . ." (Office Action, p. 5.), which does not provide any further teaching or suggestion for the claim limitations as previously stated.

Therefore, since neither Owen, Dea, nor Melo, individually or in any proper combination, teach or suggest the claim limitations "***receiving a current video frame at a dedicated video input ... directly from a video source originating the video frame, ...; computing ... a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input ...; storing the difference frame directly ... via a dedicated memory interface***" as claimed by Appellant, any combination of the cited references cannot render obvious Appellant's invention as presently claimed.

Appellant submits that since none of the references, nor any combination thereof, teach, suggest or motivate Appellant's invention as claimed in independent claim 1, the rejection should be withdrawn and claims 1 through 3, 5 through 9, and 12 and the case passed to issue.

(2) *Claims 2-9 and 12 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.*

Claims 2-9 and 12 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable. In effect, the cited references do not teach or suggest all of the claim limitations.

D. Arguments for Patentability of Claims 4 and 13 through 19

(1) *Claims 4 and 13 through 19 are patentable because the cited references do not teach or suggest all of the claim limitations.*

Regarding claim 4, Appellant respectfully asserts that claim 4 depends from independent claim 1 and reasserts the above proffered arguments in support of the allowability of independent claim 1. Appellant requests the rejection of claim 4 be withdrawn based at least on its dependency on independent claim 1.

Regarding independent claim 13, from which dependent claims 14 through 19 depend, Appellant's independent claim 13 recites:

> 13. A method for compressing video data in a computer system, comprising:
> ***receiving a current video frame at a dedicated video input*** of a core logic chip in the computer system ***directly from a video source originating the video frame***, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
> ***computing*** at the core logic chip ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;
> ***storing the difference frame directly*** from the core logic chip into the system memory in the computer system ***via a dedicated memory interface*** therebetween;
> storing the current video frame directly from the core logic chip into the system memory in the computer system using a dedicated processor interface therebetween;
> the processor retrieving the difference frame directly from the system memory via the core logic chip; and
> compressing the video data using the difference frame to produce compressed video data. (Emphasis added.)

Again, the Office Action alleges in the Response to Arguments:

Dea discloses in col. 9, lines 60-63 that "The encoding pathway receives a previous image and a current image into buffers 204, 206 respectively. The difference between the two may be applied by frame difference block 220 to selectable discrete cosine transform block 230". It is noted that previous image is current image delayed by one image. ***Thus,***

> ***the claimed "receiving a current video frame at a dedicated video input of a core logic chip ... directly from a video source originating the video frame ..." is anticipated by buffer 206 of Dea and the claimed "computing*** at the core logic chip ***a difference*** from the current video frame and a previous video frame ***as the current video frame streams into the dedicate video input*** of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, ..." ***is anticipated by frame different block 220 of Dea*** because the previous image is the current image delay by one image. (Office Action, pp. 2-3.; emphasis added).

Again, Appellant respectfully disagrees with the characterization of the teachings of Dea and Owen. Appellant's computing of a difference frame is performed in a pipelined configuration, specifically via a receiving input, namely the "dedicated video input" and a storing output, namely "a dedicated memory interface." Specifically, Appellant's invention as claimed in independent claim 13 is drawn to "***receiving a current video frame at a dedicated video input ... directly from a video source originating the video frame, ...; computing ... a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input ...; storing the difference frame directly ... via a dedicated memory interface ....***"

Again and in contrast, in the ***Owen reference***, any computing of a difference frame would need to occur in decoder/encoder 80 (FIG. 3) which is isolated by a ***single interface***, namely memory bus 167 (FIG. 3). Similarly and also in contrast to Appellant's invention as claimed, in the ***Dea reference*** teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of a ***single interface*** 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored and retrieved from memory 114.

The Office Action cites Melo et al for "teach[ing] that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be partially considered as an AGP compliant target . . ." (Office Action, p. 5.), which does not provide any further teaching or suggestion for the claim limitations as previously stated.

The Office Action cites Abramatic for "disclos[ing] the claimed step of computing an exclusive-OR between the current video frame and the previous video frame . . .." (Office Action, p. 11).

Therefore, since neither Owen, Dea, Melo, nor Abramatic nor any combination thereof, teach or suggest the claim limitations "***receiving a current video frame at a dedicated video input*** ... ***directly from a video source originating the video frame***, ...; ***computing*** ... ***a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input*** ...; ***storing the difference frame directly*** ... ***via a dedicated memory interface***" as claimed by Appellant, the cited references cannot render obvious Appellant's invention as presently claimed.

Appellant submits that since none of the references nor any combination thereof, teach, suggest or motivate Appellent's invention as claimed in independent claim 13, the rejection should be withdrawn and claims 13 through 19 and the case passed to issue.

(2) *Claims 14-19 are each allowable, among other reasons, as depending either directly or indirectly from claim 13, which is allowable.*

Claims 14-19 are each allowable, among other reasons, as depending either directly or indirectly from claim 13, which is allowable. In effect, the cited references do not teach or suggest all of the claim limitations.

(8) CLAIMS APPENDIX

LISTING OF PENDING CLAIMS:

1. (Previously Presented) A method for compressing video data in a computer system comprising:

receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;

computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;

storing the difference frame directly from the core logic chip to the system memory in the computer system via a dedicated memory interface therebetween; and

the processor retrieving the difference frame directly from the system memory via the core logic chip using a dedicated processor interface therebetween to complete compression of the video data.

2. (Previously Presented) The method of claim 1, including storing the current video frame in the system memory in the computer system.

3. (Previously Presented) The method of claim 2, wherein the current video frame is written over a previous video frame in the system memory.

4. (Original) The method of claim 1, wherein computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame.

5. (Original) The method of claim 1, wherein computing the difference frame includes computing a difference between a block of data from the current video frame and a block of data from the previous video frame.

6. (Previously Presented) The method of claim 1, wherein storing the difference frame in memory includes storing the difference frame in the system memory using block transfers.

7. (Original) The method of claim 1, including compressing the video data using the difference frame to produce compressed video data.

8. (Original) The method of claim 1, including performing a color space conversion on the video data.

9. (Original) The method of claim 1, including using the video data in compressed form in a video teleconferencing system.

10. (Cancelled).

11. (Cancelled).

12. (Original) The method of claim 1, wherein computing the difference frame

includes computing the difference frame in circuitry outside of a central processing unit in the computer system.

13. (Previously Presented) A method for compressing video data in a computer system, comprising:

receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;

computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;

storing the difference frame directly from the core logic chip into the system memory in the computer system via a dedicated memory interface therebetween;

storing the current video frame directly from the core logic chip into the system memory in the computer system using a dedicated processor interface therebetween;

the processor retrieving the difference frame directly from the system memory via the core logic chip; and

compressing the video data using the difference frame to produce compressed video data.

14. (Previously Presented) The method of claim 13, wherein the current video frame is written over a previous video frame in the system memory.

15. (Original) The method of claim 13, wherein computing the difference frame includes computing a difference between a block of data from the current video frame and a block of data from the previous video frame.

16. (Previously Presented) The method of claim 13, wherein storing the difference frame in system memory includes storing the difference frame in the system memory using block transfers.

17. (Original) The method of claim 13, including using the compressed data in a video teleconferencing system.

18. (Original) The method of claim 13, including performing a color space conversion on the video data.

19. (Previously Presented) The method of claim 13, including storing instructions and data for the computer system in the system memory.

20. (Cancelled).

(9) EVIDENCE APPENDIX

NONE

(10) RELATED PROCEEDINGS APPENDIX

NONE

CONCLUSION

Appellant respectfully requests the reversal of the rejections of currently pending claims 1-9 and 13-19 for the reasons set forth above.

Respectfully submitted,

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Date: October 31, 2005